REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated February 9, 2007, has been received and its contents carefully reviewed.

Claims 1-11, 15, 16, 18 and 20 are rejected by the Examiner. With this response, claim 5 has been amended. No new matter has been added. Claims 1-11, 15, 16, 18 and 20 remain pending in this application.

In the Office Action, claims 5-8 and 18 are rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description paragraph. Claims 1-8, 15, 16 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Related Art (hereinafter "ARA") in view of U.S. Patent No. 5,123,059 to Hirosawa et al. (hereinafter "Hirosawa"). Claims 1-11, 15, 16, 18 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,943,763 to Shibata et al. (hereinafter "Shibata") in view of Hirosawa.

With respect to the rejection of claims under 35 U.S.C. § 112, first paragraph, Applicant submits that claim 5 as amended to correct a typographic error, fully complies with 35 U.S.C. § 112, first paragraph. Accordingly, Applicant requests that the rejection to claim 5, and claims 6-8, and 18 depending from claim 5, under 35 U.S.C. § 112, first paragraph be withdrawn.

The rejection of claims 1-8, 15, 16 and 18 under 35 U.S.C. § 103(a) as being unpatentable over ARA in view of Hirosawa is respectfully traversed and reconsideration is requested. Applicant submits that ARA and Hirosawa, analyzed singly or in combination do not teach or suggest each and every element of the claims.

Independent claim 1 recites a having a combination of features including "dividing input data into most significant bit data and least significant bit data; delaying the most significant bit data for one frame period; and generating modulated current most significant bit data in accordance with a difference between the delayed most significant bit data and the current most significant bit data and independently from the least significant bit data, wherein the modulated

current most significant bit data contains more data bits than do each of the current most significant bit data and the delayed most significant bit data."

Applicant submits that ARA does not show the above combination of features. For example, ARA does not teach or suggest "generating modulated current most significant bit data in accordance with a difference between the delayed most significant bit data and the current most significant bit data and independently from the least significant bit data, wherein the modulated current most significant bit data contains more data bits than do each of the current most significant bit data and the delayed most significant bit data."

The Examiner cites FIG. 5 of Hirosawa as disclosing "wherein input data of m-bits is received by the look-up table (LUT), the look-up table modulating the input data of m-bits by outputting modulated data of n-bits where n is greater than m" to allegedly cure the deficiency in the teaching of ARA. Applicant respectfully disagrees that the teaching cited by the Examiner cures the deficiency in ARA identified above. FIG. 5 of Hirosawa teaches a lookup table receiving m-bits (the full size) of input data to produce n-bits (larger than the input data) and than the full m-bits of input data. Hirosawa then shows the n-bits of Y output from the look up table as then divided into a high order m-bits of data Y_U and lower order (n-m) bit data Y_L after the process using the look-up table is completed. See Hirosawa, FIG. 5 and column 5, lines 21-33.

Applicant submits that the modulated data and the divided data of Hirosawa does not correspond to the divided data input data and the modulated data recited in claim 1. Accordingly Applicant submits that Hirosawa does not cure the deficiencies identified above in the teachings of ARA. Applicant respectfully submits that ARA and Hirosawa, analyzed singly or in any combination, do not teach or suggest the combined features of claim 1, and that accordingly claim 1, and claims and 2-4, 15, and 16 depending from claim 1 are each allowable over ARA and Hirosawa.

Independent claim 5 recites a having a combination of features including "a modulator to modulate the most significant bits of data, the data including most significant bits of data and least significant bits of data of the n^{th} frame in accordance with a difference between the most significant bits of data for the $(n-1)^{th}$ frame and the most significant bits of data for the n^{th} frame

and independently of the least significant bits of data, wherein the modulated most significant bits of data contain more data bits than do each of the most significant bits data and the $(n-1)^{th}$ frame and the most significant bits of data for the n^{th} frame." The Examiner rejects claim 5 using similar rationale to that given for claim 1. Applicant submits that ARA and Hirosawa do not teach or suggest the quoted combination of features of claim 5 for at least the reasons given for claim 1. Accordingly, Applicant submits that claim 5 and claims 6-8 and 18 depending from claim 5 are each allowable over ARA and Hirosawa.

The rejection of claims 1-11, 15, 16, 18 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Shibata in view of Hirosawa is respectfully traversed and reconsideration is requested. Applicant submits that Shibata and Hirosawa do not teach or suggest the combined features recited in the claims.

Independent claim 1 recites a having a combination of features including "generating modulated current most significant bit data in accordance with a difference between the delayed most significant bit data and the current most significant bit data and independently from the least significant bit data." In rejecting claim 1, the Examiner cites Shibata as teaching this combination of features, in particular citing FIG. 7 and column 9, line 48 through column 11, line 42 of Shibata. Applicant respectfully disagrees with the Examiner's conclusion regarding the teachings of Shibata. Applicant submits that FIG. 7 and the cited text show that while only 5 of 8 bits stored in the frame memory, the look-up table (3) of Shibata is shown to receive all 8 bits of current (undelayed) image data to output 8 bits of data. Accordingly, Applicant submits that Shibata does not teach at least the above-quoted combination of features of claim 1. As this deficiency is not cured by the teachings of Hirosawa, Applicant submits that claim 1 is allowable over Shibata and Hirosawa for at least this reason.

Further, the Examiner acknowledges that Shibata does not teach "wherein the modulated current most significant bit data contains more data bits than do each of the current most significant bit data and the delayed most significant bit data" as recited in claim 1. The Examiner cites Hirosawa as allegedly curing this deficiency. In particular, the Examiner cites FIG. 5 of Hirosawa as disclosing "wherein input data of m-bits is received by the look-up table (LUT), the look-up table modulating the input data of m-bits by outputting modulated data of n-bits where n is greater than m" as recited in claim 1 to allegedly cure the deficiency in the

teaching of Shibata. Applicant respectfully disagrees that the Hirosawa, including the portions cited by the Examiner cures the deficiencies in the teachings of Shibata with respect to the features recited in claim 1.

FIG. 5 of Hirosawa teaches a lookup table receiving m-bits (the full size) of input data to produce n-bits (larger than the input data) and than the full m-bits of input data. Hirosawa then shows the n-bits of Y output from the look up table as then divided into a high order m-bits of data Y_U and lower order (n-m) bit data Y_L after the process using the look-up table is completed. See Hirosawa, FIG. 5 and column 5, lines 21-33.

Applicant submits that the modulated data and the divided data of Hirosawa does not correspond to the divided data input data and the modulated data recited in claim 1. Accordingly Applicant submits that Hirosawa does not cure the deficiencies identified above in the teachings of Shibata. Applicant respectfully submits that Shibata and Hirosawa, analyzed singly or in any combination, do not teach or suggest the combined features of claim 1, for at least this additional reason. Accordingly, Applicant respectfully submits that claim 1, and claims and 2-4, 15, and 16 depending from claim 1 are each allowable over ARA and Hirosawa.

Independent claim 5 recites a driving apparatus for a liquid crystal display having a combination of features including "a modulator to modulate the most significant bits of data, the data including most significant bits of data and least significant bits of data of the n^{th} frame in accordance with a difference between the most significant bits of data for the $(n-1)^{th}$ frame and the most significant bits of data for the n^{th} frame and independently of the least significant bits of data." The Examiner cites Shibata as teaching this combination of features, in particular citing FIG. 7 and column 9, line 48 through column 11, line 42 of Shibata." Applicant submits that Shibata does not teach or suggest "a modulator to modulate the most significant bits of data ... independently of the least significant bits of data" or "wherein the modulated most significant bits of data contain more data bits than do each of the most significant bits data and the $(n-1)^{th}$ frame and the most significant bits of data for the n^{th} frame" for the same reasons given for claim 1 above. Accordingly, Applicant respectfully submits that Shibata and Hirosawa do not teach or suggest this features of claim 5 for at least the reasons given for claim 1 and that claim 5 and claims 6-8 and 18 depending from claim 5 are each allowable over ARA and Hirosawa.

Independent claim 9 recites a liquid crystal display having a combination of features including "a data modulator to modulate the most significant bits of the RGB data based on a look-up table storing modulated most significant bits of the RGB data, wherein the modulated most significant bits of the RGB data contain more data bits than do the most significant bits of the RGB data and wherein the least significant bits of the RGB data bypass the modulator." In rejecting claim 9, the Examiner cites FIG. 7 of Shibata as disclosing "wherein the least significant bits of the RGB data bypass the modulator," specifically identifying blocks (2, 3) as showing "bypass the modulator. Applicant respectfully disagrees with the Examiner's conclusion regarding the teaching of Shibata. In describing the operation of the "data comparing and corrected data generating means 3", Shibata states the following at column 10, lines 31-40:

> "If a look-up table for reading out corrected data according to the relationship between the previous image data and the current image data is used as the data comparing and corrected data generating means 3, then the capacity of the look-up table required for comparing the most significant 5 bits of each RGB element of the previous image data with the respective 8-bit RGB elements of the current image data, in order to generate respective 5-bit RGB corrected data, will be 3 x 32 x 256 * 5 = 3 * 40 Kbit = 120 Kbit and hence the memory capacity can be reduced compared to the prior art..."

Applicant submits that FIG. 7 and the above text of Shibata disclose using all 8 bits of the "current image data" to generate "corrected data" as some function of the "current image data" and accordingly do not teach or suggest "wherein the least significant bits of the RGB data bypass the modulator" as recited in claim 9.

Additionally, the Examiner further acknowledges that Shibata does not teach or suggest "wherein the modulated most significant bits of the RGB data contain more data bits than do the most significant bits of the RGB data" as recited in claim 9.

The Examiner cites Hirosawa as disclosing "wherein the m bits of input data is received by a look up table (LUT) the look up table modulating the input data of m-bits by outputting data of n-bits" to allegedly cure the deficiency in Shibata regarding "wherein the modulated most significant bits of the RGB data contain more data bits than do the most significant bits of the RGB data" as recited in claim 9. Applicant respectfully disagrees that Hirosawa, including the portions cited by the Examiner, cures this deficiencies in the teachings of Shibata for reasons similar to those given above with respect to claim 1. Accordingly, Applicant respectfully

submits that as Shibata and Hirosawa, analyzed singly or in combination do not teach or suggest the combined features of claim 9, claim 9 and claims 10, 11, and 20 depending from claim 9 are each allowable over Shibata and Hirosawa.

Applicant believes the foregoing amendments and remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. *A duplicate copy of this sheet is enclosed.*

Respectfully submitted,

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By _____ 40,106

Valerie P. Hayes
Registration No. 53,005
McKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorneys for Applicant